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09/586,961	06/05/2000	Akihiko Ohwada	1341.1048/JDH	8507

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	6

DATE MAILED: 12/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/586,961	OHWADA, AKIHIKO	
	Examin r	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☒ Interview Summary (PTO-413) Paper No(s). *6*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-10 have been cancelled per Applicant's request. New claims 11-26 have been added and considered. Claims 17, 20, and 22 claim dependencies have been amended as per Applicant's representative's indication in a telephone interview on 20 November 2003. The interview summary is attached.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 11-12, 14-16, 18-20, 22-24, and 26 are rejected under 35 U.S.C. 102(e) as being taught by Lynch, U.S. Patent Number 5,930,492 (herein referred to as Lynch).

4. Referring to claim 11, Lynch has taught a processor execution pipeline, comprising:

   a. A first instruction decoding unit that decodes a first instruction into a first control signal, and decodes instructions with the exception of the first instruction into a second control signal (Lynch column 2, lines 4-58; column 21, line 15 to column 22, line 40; column 22, line 66 to column 23. line 46; Figure 6; Figure 7; Figure 8; Figure 9; and Figure 10). In regards to Lynch, the control word and steering work essentially functions similar to the instruction decoder, since they provide the control signals to the processing unit and other hardware in the pipeline stage.

Also, a simple decoder is inherent to the stage to decode the control word by isolating the control field in the control word used for that particular stage.

b. A first processing unit that performs a first operation on a first data when receiving the first control signal, and passes the first data when receiving the second control signal (Lynch column 22, lines 41-65; Figure 6; Figure 7; and Figure 9);

c. A second instruction decoding unit that decodes a second instruction into a third control signal, and decodes instructions with the exception of the second instruction into a fourth control signal (Lynch column 2, lines 4-58; column 21, line 15 to column 22, line 40; column 22, line 66 to column 23. line 46; Figure 6; Figure 7; Figure 8; Figure 9; and Figure 10). In regards to Lynch, the control word and steering work essentially functions similar to the instruction decoder, since they provide the control signals to the processing unit and other hardware in the pipeline stage. Also, a simple decoder is inherent to the stage to decode the control word by isolating the control field in the control word used for that particular stage.

d. A second processing unit that performs a second operation on a second data when receiving the third control signal where the second data is an output of the first processing unit (Lynch column 22, lines 41-65; Figure 6; Figure 7; and Figure 9); and

e. A multiplexer that selects an output of the second processing unit or the second data (Lynch column 20, line 20 to column 21, line 14; column 22, line 41 to column 23, line 13; Figure 6; and Figure 9).

5. Referring to claim 12, Lynch has taught wherein the multiplexer selects an output of the second processing unit when receiving the third control signal, and selects the second data when receiving the fourth control signal (Lynch column 20, line 20 to column 21, line 14; column 22, line 41 to column 23, line 13; Figure 6; and Figure 9).

6. Referring to claim 14, Lynch has taught wherein the first processing unit receives multiple data as the first data (Lynch column 22, line 41 to column 23, line 50; and Figure 9).

7. Referring to claim 15, Lynch has taught a processor execution pipeline, comprising:

a. A first instruction decoding unit that decodes a first instruction into a first control signal, and decodes instructions with the exception of the first instruction into a second control signal (Lynch column 2, lines 4-58; column 21, line 15 to column 22, line 40; column 22, line 66 to column 23. line 46; Figure 6; Figure 7; Figure 8; Figure 9; and Figure 10). In regards to Lynch, the control word and steering work essentially functions similar to the instruction decoder, since they provide the control signals to the processing unit and other hardware in the pipeline stage. Also, a simple decoder is inherent to the stage to decode the control word by isolating the control field in the control word used for that particular stage.

b. A first processing unit that performs a first operation on a first data when receiving the first control signal (Lynch column 22, lines 41-65; Figure 6; Figure 7; and Figure 9);

c. A multiplexer that selects an output of the first processing unit or the first data (Lynch column 20, line 20 to column 21, line 14; column 22, line 41 to column 23, line 13; Figure 6; and Figure 9);

d. A second instruction decoding unit that decodes a second instruction into a third control signal, and decodes instructions with the exception of the second instruction into a fourth control signal (Lynch column 2, lines 4-58; column 21, line 15 to column 22, line 40; column 22, line 66 to column 23. line 46; Figure 6; Figure 7; Figure 8; Figure 9; and Figure 10). In regards to Lynch, the control word and steering work essentially functions similar to the instruction decoder, since they provide the control signals to the processing unit and other hardware in the pipeline stage. Also, a simple decoder is inherent to the stage to decode the control word by isolating the control field in the control word used for that particular stage.

e. A second processing unit that performs a second operation on a second data when receiving the third control signal, and passes the second data when receiving the fourth control signal, where the second data is an output of the multiplexer (Lynch column 22, lines 41-65; Figure 6; Figure 7; and Figure 9).

8. Referring to claim 16, Lynch has taught wherein the multiplexer selects an output of the first processing unit when receiving the first control signal, and selects the first data when receiving the second control signal (Lynch column 20, line 20 to column 21, line 14; column 22, line 41 to column 23, line 13; Figure 6; and Figure 9).

9. Referring to claim 18, Lynch has taught wherein the first processing unit receives multiple data as the first data, and the multiplexer receives the output of the first operating unit and one of the multiple data (Lynch column 22, line 41 to column 23, line 50; and Figure 9).

10. Referring to claim 19, Lynch has taught a processor execution pipeline, comprising:

a. A first instruction decoding unit that decodes a first instruction into a first control signal, and decodes instructions with the exception of the first instruction into a second control signal (Lynch column 2, lines 4-58; column 21, line 15 to column 22, line 40; column 22, line 66 to column 23. line 46; Figure 6; Figure 7; Figure 8; Figure 9; and Figure 10). In regards to Lynch, the control word and steering work essentially functions similar to the instruction decoder, since they provide the control signals to the processing unit and other hardware in the pipeline stage. Also, a simple decoder is inherent to the stage to decode the control word by isolating the control field in the control word used for that particular stage.

b. A first processing unit that performs a first operation on a first data when receiving the first control signal, and passes the first data when receiving the second control signal (Lynch column 22, lines 41-65; Figure 6; Figure 7; and Figure 9);

c. A second instruction decoding unit that decodes the first instruction into a third control signal, decodes a second instruction into a fourth control signal, and decodes instructions with the exception of the first and second instructions into a fifth control signal (Lynch column 2, lines 4-58; column 21, line 15 to column 22, line 40; column 22, line 66 to column 23. line 46; Figure 6; Figure 7; Figure 8;

Figure 9; and Figure 10). In regards to Lynch, the control word and steering work essentially functions similar to the instruction decoder, since they provide the control signals to the processing unit and other hardware in the pipeline stage. Also, a simple decoder is inherent to the stage to decode the control word by isolating the control field in the control word used for that particular stage.

d. A second processing unit that performs a second operation on a second data when receiving the third control signal, and performs a third operation on the second data when receiving the fourth control signal, where the second data is an output of the first processing unit (Lynch column 22, lines 41-65; Figure 6; Figure 7; and Figure 9); and

e. A multiplexer that selects an output of the second processing unit or the second date (Lynch column 20, line 20 to column 21, line 14; column 22, line 41 to column 23, line 13; Figure 6; and Figure 9).

11. Referring to claim 20, Lynch has taught wherein the multiplexer selects an output of the second processing unit when receiving either one of the third or the fourth control signals, and selects the second data when receiving the fifth control signal (Lynch column 20, line 20 to column 21, line 14; column 22, line 41 to column 23, line 13; Figure 6; and Figure 9).

12. Referring to claim 22, Lynch has taught wherein the first processing unit receives multiple data as the first data (Lynch column 22, line 41 to column 23, line 50; and Figure 9).

13. Referring to claim 23, Lynch has taught a processor execution pipeline, comprising:

a. A first instruction decoding unit that decodes a first instruction into a first control signal, decodes a second instruction into a second control signal, and decodes

instructions with the exception of the first and second instructions into a third control signal (Lynch column 2, lines 4-58; column 21, line 15 to column 22, line 40; column 22, line 66 to column 23. line 46; Figure 6; Figure 7; Figure 8; Figure 9; and Figure 10). In regards to Lynch, the control word and steering work essentially functions similar to the instruction decoder, since they provide the control signals to the processing unit and other hardware in the pipeline stage. Also, a simple decoder is inherent to the stage to decode the control word by isolating the control field in the control word used for that particular stage.

b. A first processing unit that performs a first operation on a first data when receiving the first control signal, and performs a second operation on the first data when receiving the second control signal (Lynch column 22, lines 41-65; Figure 6; Figure 7; and Figure 9);

c. A multiplexer that selects an output of the first processing unit or the first data (Lynch column 20, line 20 to column 21, line 14; column 22, line 41 to column 23, line 13; Figure 6; and Figure 9);

d. A second instruction decoding unit that decodes the first instruction into a fourth control signal, and decodes instructions with the exception of the first instruction into a fifth control signal (Lynch column 2, lines 4-58; column 21, line 15 to column 22, line 40; column 22, line 66 to column 23. line 46; Figure 6; Figure 7; Figure 8; Figure 9; and Figure 10). In regards to Lynch, the control word and steering work essentially functions similar to the instruction decoder, since they provide the control signals to the processing unit and other hardware in the

pipeline stage. Also, a simple decoder is inherent to the stage to decode the control word by isolating the control field in the control word used for that particular stage.

e. A second processing unit that performs a third operation on a second data when receiving the fourth control signal, and passes the second data when receiving the fifth control signal, where the second data is an output of the multiplexer (Lynch column 22, lines 41-65; Figure 6; Figure 7; and Figure 9).

14. Referring to claim 24, Lynch has taught wherein the multiplexer selects an output of the first processing unit when receiving either one of the first or the second control signals, and selects the first data when receiving the third control signal (Lynch column 20, line 20 to column 21, line 14; column 22, line 41 to column 23, line 13; Figure 6; and Figure 9).

15. Referring to claim 26, Lynch has taught wherein the first processing unit receives multiple data as the first data, and the multiplexer receives the output of the first operating unit and one of the multiple data (Lynch column 22, line 41 to column 23, line 50; and Figure 9).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 13, 17, 21, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lynch, as applied to claims 11, 15, 19, and 23 above, in view of InstantWeb's Free Online Computing Dictionary (herein referred to as FOLDOC). Lynch has not explicitly taught a

latching unit that holds the output of the first processing unit where the second data is data held by the latching unit. However, Lynch has taught that the dataflow elements, which include the dataflow element the second data passes through at the end of a stage, may be arithmetic/logical dataflow elements, data routing elements, or storage devices. FOLDOC has taught a latching unit that holds data (FOLDOC Latch). A person of ordinary skill at the time the invention was made would have recognized that a latch is a type of storage device and, when used as a dataflow element from Lynch, holds the output of the first processing unit where the second data is data held by the latching unit until the next stage is ready. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the latch of FOLDOC in the device of Lynch to ensure the data available and ready when the next stage is ready.

Response to Arguments

18. Applicant's arguments with respect to claims 11-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Petolino, Jr., U.S. Patent Number 5,928,355, has taught a pipeline with data bypassing and latches.

b. Biswas et al., U.S. Patent Number 6,012,139, has taught a pipeline with data bypassing and latches.

c. McLellan, U.S. Patent Number 5,325,495, has taught a pipeline with data bypasses and latches.

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

21. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

23. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

24. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

November 25, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100